REMARKS

The title has been amended as recommended by the Examiner.

The abstract has been amended and placed on a separate sheet of paper as recommended by the Examiner.

Claims 19 and 21-26 are pending. Claims 22, 24 and 25 are not canceled, but have been withdrawn from consideration pending determination of allowability of the generic claims.

Claims 19, 21, 23 and 26 have been rejected under 35 USC 103(a) as being unpatentable over U.S. patent 5,483,421 ("Gedney") in view of U.S. patent 5,680,936 ("Beers"). Applicants respectfully traverse this rejection in view of the amended claims for the following five reasons, each of which is an independent reason that is individually sufficient to justify allowance of the claims:

1) Independent claim 19 recites testing multiple semiconductor dice on a multi-chip subassembly with at least one passive component, then coupling the subassembly to a substrate if the test passes. Neither Gedney nor Beers discloses or suggests connecting a subassembly to a substrate based on the results of testing the subassembly. Neither Gedney nor Beers discloses or suggests any kind of assembly process that is conditioned on test results. Gedney does not discuss the subject of testing at all. Beers separates tested printed circuit boards into those that passed the testing and those that did not, but does nothing further with the boards. The rejection implies that the claimed limitations may be read into the references because these limitations produce beneficial results such

as customer satisfaction. Beneficial results do not equate to obviousness - if they did, few if any patents would ever be granted.

2) Independent claim 19 recites coupling a successfully tested subassembly to a substrate with solder balls. Only Beers discusses testing at all, and Beers only deals with testing completed printed circuit boards. Since the use of solder balls is a technique that is used on integrated circuits but not on printed circuit boards, it would not be obvious to implement this technique on the tested printed circuit boards of Beers.

3) Independent claim 19 recites soldering the tested subassembly to a substrate and coupling another integrated circuit device to the substrate. At most, the printed circuit boards of Beers might be plugged into the connectors on a motherboard (something that might be suggested in other references but is not suggested by Beers and Gedney), but would not be soldered to a substrate having other integrated circuits on it.

4) Beers tests a completed printed circuit board. At most, the printed circuit board of Beers would contain multi-chip subassemblies that had already been attached to the printed circuit board before Beers begins testing, which is contrary to the claims and which represents the problematic prior art approach that Applicant's invention is intended to overcome.

5) Gedney and Beers involve completely different devices at completely different stages of the manufacturing process. Combing them in the manner suggested would not be feasible because the techniques of Gedney are not applicable to the processes of Beers, and the techniques of Beers are not applicable to the processes of Gedney.

Claims 21-26 depend from claim 19 and therefore contain the same limitations not disclosed or suggested by the cited references. Claims 21 and 23 have been amended

only to provide consistency with the terminology of amended claim 19. Claims 22, 25 and 26 are not currently under consideration, but will be similarly amended for consistent terminology as necessary once the other pending claims have been allowed.

CONCLUSION

For the aforementioned reasons, Applicants maintain that claims 19, 21, 23 and 26 are now in condition for allowance. Applicants further maintain that since generic claim 19 is in condition for allowance, claims 22, 24 and 25 should now be considered by the Examiner. No fee is believed due with this response. In this is incorrect, please charge any insufficiency or credit any overpayment to Deposit Account No. 02-2666.

Respectfully submitted,

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APPENDIX A

MARKED-UP COPY OF AMENDED CLAIMS

19. (Amended four times) A method of assembling a multi-chip device comprising:

providing an interposer having a first surface and a second surface;

populating the second surface with a plurality of conductive pads;

coupling a solder ball to each of selected ones of the plurality of conductive pads;

coupling [at least one] a plurality of semiconductor [die] dice and at least one passive device to the first surface to form a multi-chip subassembly, wherein the at least one passive device is selected from a group comprising resistors, capacitors, and inductors;

testing said [at least one semiconductor die] plurality of semiconductor dice on said interposer; [and]

coupling said interposer to a substrate with the solder balls after said testing if said [at least one semiconductor die] plurality of semiconductor dice passes said testing; and

coupling at least one other semiconductor device to the substrate.

21. (Amended twice) The method of claim 19 wherein [fabricating] providing comprises [fabricating] providing the interposer [with] having organic material.

23. (Amended three times) The method of claim 19 further comprising not coupling said interposer to the substrate if said [at least one semiconductor die] plurality of semiconductor dice does not pass said testing.